Claims:

Claims 1-21 are pending in the application.

1.(original) A method for performing a transaction on a bus, comprising:

receiving a signal requesting the transaction;

generating a first value using the signal;

storing the first value in a storage device, with the first value including a plurality of bits indicating a beginning of usage of the bus and an ending of the usage of the bus for the transaction in terms of clock cycles; and

executing the transaction according to the first value.

2.(original) The method as recited in claim 1, wherein:

storing the first value in the storage device includes storing the plurality of bits in storage elements included in the storage device, with those of the plurality of bits in a first state indicating the clock cycles during which the usage of the bus occurs for the transaction.

3.(original) The method as recited in claim 2, wherein:

each of the storage elements stores one of the plurality of bits.

4.(original) The method as recited in claim 3, wherein:

receiving the signal includes receiving a second value indicating a number of the clock cycles during which the usage of the bus occurs for the transaction;

generating the first value includes generating the plurality of bits using the second value with positions within the first value of those of the plurality of bits in the first state indicating the clock cycles during which the usage of the bus occurs for the transaction; and

each of the positions within the first value corresponds to one of the storage elements.

5.(original) The method as recited in claim 4, further comprising:

changing the first value in the storage device after storing the first value and after an occurrence of at least one of the clock cycles by shifting ones of the plurality of bits between the storage elements.

6.(original) The method as recited in claim 5, wherein:

executing the transaction includes monitoring a first one of the positions to determine a beginning of the transaction.

7.(original)The method as recited in claim 6, wherein:

those of the plurality of bits in a second state indicate the clock cycles during which the bus exists in an idle condition; and

generating the first value includes generating the plurality of bits in the second state so that the bus exists in the idle condition for at least one of the clock cycles between the usage of the bus for the transaction and the usage of the bus for a previous transaction.

8.(original)The method as recited in claim 7, wherein:

the bus includes a data bus;

the transaction includes an access to a memory device including a control phase and a data phase;

executing the transaction includes beginning the control phase when the first one of the positions enters the second state; and

executing the transaction includes beginning the data phase when a second one of the positions enters the first state.

9.(original)The method as recited in claim 7, wherein:

the bus includes an address bus;

the transaction includes an access to a memory device including a control phase;

executing the transaction includes beginning the control phase when the

the first one of the positions enters the first state.

10.(original) A system, comprising:

a bus;

a processor configured to receive first data from the bus;

a first memory device configured to send the first data to the bus;

a memory controller coupled to the processor and the memory device and configured to control transfer of the first data over the bus; and

a bus management device arranged to receive a first value from the memory controller indicating a number of clock cycles with the first data on the bus and including a storage device to store a second value including a first plurality of bits for indicating a beginning of the first data on the bus and an ending of the first data on the bus in terms of the clock cycles.

11.(original) The system as recited in claim 10, wherein:

the storage device includes storage elements for storing the first plurality of bits, with positions within the second value of those of the first plurality of bits in a first state indicating the clock cycles during which the first data exists on the bus; and

the bus management device includes a configuration to change the second value by shifting ones of the first plurality of bits between the storage elements after an occurrence of at least one of the clock cycles.

12.(original) The system as recited in claim 11, wherein:

those of the first plurality of bits in a second state indicate the clock cycles during which the bus exists in an idle condition; and

the bus management device includes a configuration to detect a change in one of the positions within the second value from the first state to the second state and to signal the memory controller to begin a first access to the first memory device a first time period before the clock cycles corresponding to those of the first plurality of bits in the first state begin.

13.(original) The system as recited in claim 12, further comprising:

a second memory device configured to send second data to the bus, with the processor configured to receive the second data from the bus and with the bus

management device arranged to receive a third value from the memory controller indicating a number of the clock cycles with the second data on the bus and to store a fourth value in the storage elements including a second plurality of bits for indicating a beginning of the second data on the bus and an ending of the second data on the bus in terms of the clock cycles.

14. (original) The system as recited in claim 13, wherein:

positions within the fourth value of those of the second plurality of bits in the first state indicate the clock cycles during which the second data exists on the bus; and

the bus management device includes a configuration to change the fourth value by shifting ones of the second plurality of bits between the storage elements after an occurrence of at least one of the clock cycles.

15.(original) The system as recited in claim 14, wherein:

those of the second plurality of bits in the second state indicate the clock cycles during which the bus exists in an idle condition; and

the bus management device includes a configuration to detect a change in one of the positions within the fourth value from the first state to the second state and to signal the memory controller to begin a second access to the second memory device a second time period before the clock cycles corresponding to those of the second plurality of bits in the first state begin.

16.(original) An electrophotographic imaging device for forming images on media using imaging data, comprising:

a photoconductor;

a photoconductor exposure system configured to generate a latent electrostatic image on the photoconductor using video data;

a video data generator configured to generate the video data using pixel data;

a processor configured to generate the pixel data from the imaging data;

a bus;

a first memory device configured to provide first data to the bus;

a memory controller configured to control transfer of the first data between the first memory device and the processor; and

a bus management device arranged to receive a first value from the memory controller indicating a number of clock cycles with the first data on the bus and including a storage device to store a second value including a first plurality of bits for indicating a beginning of the first data on the bus and an ending of the first data on the bus in terms of the clock cycles.

17.(original) The electrophotographic imaging device as recited in claim 16, wherein:

the storage device includes a register with positions within the register of those of the first plurality of bits in a first state indicating the clock cycles during which the first data exists on the bus; and

the bus management device includes a configuration to change the second value by shifting ones of the first plurality of bits in the register after an occurrence of one of the clock cycles.

18.(original) The electrophotographic imaging device as recited in claim 17, wherein:

the bus management device includes a configuration to signal the memory controller to begin a first control phase of a first access to the first memory device after storing the second value in the register and a configuration to generate the second value from the first value so that substantially contemporaneous with completion of the first control phase the clock cycles corresponding to those of the first plurality of bits in the first state begin.

19.(original) The electrophotographic imaging device as recited in claim 18, further comprising:

a second memory device configured to send second data to the bus, with the memory controller configured to control transfer of the second data between the

second memory device and the processor and with the bus management device arranged to receive a third value from the memory controller indicating a number of clock cycles with the second data on the bus and configured to store a fourth value including a second plurality of bits for indicating a beginning of the second data on the bus and an ending of the second data on the bus in terms of the clock cycles.

20.(original) The electrophotographic imaging device as recited in claim 19, wherein:

the bus management device includes a configuration to change the fourth value by shifting ones of the first plurality of bits in the register after an occurrence of one of the clock cycles; and

the bus management device includes a configuration to signal the memory controller to begin a second control phase of a second access to the second memory device after storing the fourth value in the register and a configuration to generate the fourth value from the third value so that substantially contemporaneous with completion of the second control phase the clock cycles corresponding to those of the second plurality of bits in the first state begin; and

a number of the clock cycles forming the first control phase differs from a number of clock cycles forming the second control phase.

21.(original) The electrophotographic imaging device as recited in claim 20, wherein:

the bus management device includes a configuration to generate and to store the fourth value in the register so that one of the clock cycles occurs between those of the first plurality of bits in the first state and those of the second plurality of bits in the first state.